UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,323	12/31/2001	Philip L. Hower	TI-30010	3224

23494 7590 01/29/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 200401

Application Number: 10/036,323

Filing Date: December 31, 2001

Appellant(s): HOWER ET AL.

Thomas L. Dickey

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/22/03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because it leaves out six limitations, yet adds a limitation not found in the claims.

Limitations found in the claims but not in the summary of invention contained in the brief include:

1) A conductive gate structure
2) A source metallization
3) An ohmic connection between the buried body and the source metallization
4) An ohmic connection between the source region and the source metallization
5) Capacitive coupling between the gate and part of the p body
6) Functional limitation that the buried body be capable of diverting hole current from the source region in order to reduce emission of secondary holes.

The limitation added to the summary of invention contained in the brief but not found in the claims is that the channel region is formed directly beneath the gate.

For a correct summary of the invention the reader should reference figures 4G and 4H as that figure was amended on February 10, 2003.

The invention is an n-channel DMOS transistor that includes source metallization 419 (this part appears only in figure 4H) , n-type source diffusion 18, p-type surface body diffusion 20, a conductive gate structure 24 (number appears only in figure 4G) and p-type buried body diffusion 30. The source metallization 419 must be ohmically connected to both the n-type source diffusion 18 and the p-type buried body diffusion 30. P-type surface body diffusion 20 must laterally surround at least part of n-type source diffusion 18. P-type buried body diffusion 30 must be capable of diverting hole current from the source region in order to reduce emission of secondary holes. Conductive gate structure 24 and p-type surface body diffusion 20 must be capacitively coupled in such a way as to define a channel region in part of p-type surface body diffusion 20, and p-type buried body diffusion 30 must underlie the part of p-type surface body diffusion 20 defined as said channel region.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 14,16, and 18 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,922,327	MENA et al.	5-1990
6,437,399	HUANG	12-2003
4,922,327	MENA et al.	5-1990

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 14 stands rejected under 35 U.S.C. 102(e) as being anticipated by HUANG (6,437,399). Huang discloses an n-channel DMOS transistor source structure comprising an n-type source diffusion 16, ohmically connected to a source metallization 36, a p-type surface body diffusion 14 which laterally surrounds at least part of said source diffusion 16, a conductive gate structure 26 which is capacitively coupled to part of said p-type surface body diffusion 14 to define a channel region therein, a p-type buried body diffusion 35 which underlies said channel and at least part of said surface body diffusion 14; and an ohmic connection between said buried body

diffusion 35 and said source metallization 36; whereby said buried body diffusion 35 is capable of diverting hole current to bypass said source diffusion 16, and thereby reducing emission of secondary electrons, and thereby increasing the safe operating area of the device. Note figure 12 and column 2 lines 40-43 and column 3 lines 5-8 of Huang.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over HUANG (6,437,399) in view of MENA ET AL. (4,922,327).

With regard to claim 16, Huang discloses an n-channel DMOS transistor source structure comprising an n-type source diffusion 16, ohmically connected to a source metallization 36, a p-type surface body diffusion 14 which laterally surrounds at least part of said source diffusion 16, a conductive gate structure 26 which is capacitively coupled to part of said p-type surface body diffusion 14 to define a channel region therein, a p-type buried body diffusion 35 which underlies said channel and at least part of said surface body diffusion 14; and an ohmic connection between said buried body diffusion 35 and said source metallization 36; whereby said buried body diffusion 35 diverts hole current to bypass said source diffusion 16, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the

device. Note figure 12 and column 2 lines 40-43 and column 3 lines 5-8 of Huang. Huang does not disclose that the n-channel DMOS transistor source structure comprises a drain region that is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor. However, Mena et al. discloses an n-channel DMOS transistor source structure comprising a drain region 24 that is laterally spaced from a channel 20 by a drift region 22a, to thereby define a lateral DMOS transistor. Note figure 1 of Mena et al. Therefore, it would have been obvious to a person having skill in the art to replace the vertical drain of Huang's n-channel DMOS transistor source structure with the drain region which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor such as taught by Mena et al. in order to maintain a relatively high breakdown voltage while exhibiting a relatively low on-resistance, and preventing parasitic breakdown in a LDMOS.

With regard to claim 18, Huang discloses an n-channel DMOS transistor source structure comprising an n-type source diffusion 16, ohmically connected to a source metallization 36, a p-type surface body diffusion 14 which laterally surrounds at least part of said source diffusion 16, a conductive gate structure 26 which is capacitively coupled to part of said p-type surface body diffusion 14 to define a channel region therein, a p-type buried body diffusion 35 which underlies said channel and at least part of said surface body diffusion 14; and an ohmic connection between said buried body diffusion 35 and said source metallization 36; whereby said buried body diffusion 35 diverts hole current to bypass said source diffusion 16, and thereby reduces emission of secondary electrons, and thereby increases the safe operating area of the device. Note figure 12 and column 2 lines 40-43 and column 3 lines 5-8 of Huang. Huang does

not disclose that the n-channel DMOS transistor source structure further comprises a drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor. However, Mena et al. discloses an n-channel DMOS transistor source structure comprising a drain structure 116-128-140 which includes at least one shallow n-well diffusion 128 laterally surrounding an n+ drain diffusion 140, and which is laterally spaced from said channel by a drift region 116, to thereby define a lateral DMOS transistor. Note figures 4-7 of Mena et al. Therefore, it would have been obvious to a person having skill in the art to replace the vertical drain of Huang's n-channel DMOS transistor source structure with the drain structure which includes at least one shallow n-well diffusion laterally surrounding an n+ drain diffusion, and which is laterally spaced from said channel by a drift region, to thereby define a lateral DMOS transistor such as taught by Mena et al. in order to maintain a relatively high breakdown voltage while exhibiting a relatively low on-resistance, and preventing parasitic breakdown in a LDMOS.

(11) Response to Argument

As an initial matter, at the bottom of page three of Applicants' brief Applicants state "It should also be noted that claim 14 comprises the limitation of p-type surface body diffusion and a separate 'channel region.'" This statement simply misstates the plain language of claim 14. Lines 5 and 6 of claim 14 read in pertinent part "coupled to part of said p-type surface body diffusion to define a channel region therein." The last word, "therein," relates back to "said p-type surface body diffusion." The word "therein" means "within." By the plain language of the claim, the

channel region is not separate from the p-type surface body diffusion because the claim requires the channel region to be formed within the p-type surface body diffusion.

Appellants contend that claim 14 was not properly rejected because it uses an overbroad definition of the term "channel region" as used in claim 14 of the instant invention. On page three of their brief Applicants state

The 'channel region' of the instant invention is ... formed when the appropriate voltages are applied to the conductive gate structure and [therefor the 'channel region'] will be confined by the existing electric fields to regions directly beneath the conductive gate structure. This definition of 'channel region' coincides with the well-established use of the term in semiconductor physics. Appendix I contain the pages from 'Physics of Semiconductor Devices' by Sze, which provide an explanation of the formation of the 'channel region' and its confinement to regions beneath the conductive gate. In particular pages 433 to 445 provide the physics behind the formation of the 'channel region' and Fig. 3[1] and Fig. 6[2] show the confinement of the 'channel region' to the region directly beneath the conductive gate. This is also illustrated in Fig. 19[3] where the 'channel region' is shown for various types of transistors.

The examiner agrees that in an n-MOSFET, when the voltage on the gate exceeds the threshold voltage, an n-type surface inversion layer (some call this a channel, as Sze points out on page 434 of Applicants' reference) forms. However, the examiner takes the position that if it were critical to the invention for the p-type buried body to be formed under the n-type surface inversion layer, this critical information should have been introduced in Applicants' specification

---

[1] Here applicants refer to figure 3 of Sze. Figure 3 of the instant application does not show a 'channel region' confined to regions below a conductive gate.

[2] Applicants refer to figure 6 of Sze. Figure 6 of the instant application does not show a 'channel region' confined to regions below a conductive gate.

[3] Once again, Applicants refer to figure 19 of Sze. There is no figure in the instant application that shows the configuration Applicants herein "borrow" from Sze.

and not withheld until the eleventh hour and supplied as an attachment to applicants' appeal brief.

Furthermore, none of applicants' original statements concerning the "channel region" in the specification support defining "channel region" as the n-type surface inversion layer disclosed by Sze. For example:

On page 5 line 25 Applicants state that the buried body is placed beneath the source and p-type body. No mention of channels.

On page 8 line 22 Applicants state that the channel region is of first conductivity type, the opposite type from the second conductivity type source (page 8 line 26). If "channel region" were synonymous with Sze's n-type surface inversion layer (as Applicants have taken this late opportunity to assert), this statement would make no sense, since Sze's n-type surface inversion layer is the same type, not opposite, to the conductivity type of the source.

On page 9 line 2 Applicants state the "A gate 24 covers at least a portion of the channel region," in other words, that the gate need not cover all of the "channel region." The implication is that the "channel region" is not intimately associated with the gate.

On page 9 lines 11-12 Applicants state that the buried p-diffusion 30 should be proximate the source 18 and preferably under the source 18. No mention of a requirement that the buried p-diffusion 30 should be under an n-type surface inversion layer, or channel.

On pages 10 and 11 Applicants state that they built an experimental LDMOS, and that the experimental LDMOS showed improvements illustrated in figures 2A and 2B. Nowhere do

applicants state that the experimental LDMOS in question had a buried p-body that extended under an n-type surface inversion layer, or channel, adjacent to a gate.

On page 14 lines 8-16 applicants state that the source, surface body, and buried body should be formed in a triple implant through the same mask window so that the buried body is "self-aligned" with the source. The implication is that the buried body is formed below the source and nowhere else.

The examiner believes that the correct way to define "channel region" is to give it the broadest meaning derivable from the plain language of the claim that is consistent with the specification. From the plain language of the claim, the channel region is part (any part up to practically all) of the p-type surface body diffusion that is capacitively coupled to the gate. Note claim 14 lines 5-6. In Huang et al.6,437,399 (as long as gate 26 is not supplied with a voltage large enough to cause an inversion layer to form) practically the entire body region 14, including the part that overlies p-type buried body diffusion 35, is capacitively coupled to gate 26. Therefore, the broadest reading of "channel region," consistent with the plain meaning of claim 14, results in claim 14 reading on Huang et al.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thomas L. Dickey

January 12, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conferees:

Nathan Flynn

Olik Chaudhuri

Thomas L. Dickey

TEXAS INSTRUMENTS INCORPORATED

P O BOX 655474, M/S 3999

DALLAS, TX 75265